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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/684,611	10/06/2000	Guy Meynants	M-11283 US	3244
7590	05/05/2005		EXAMINER	
Jack V Musgrove 10921 SIERRA OAKS AUSTIN, TX 78759			LONG, HEATHER R	
			ART UNIT	PAPER NUMBER
			2615	

DATE MAILED: 05/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/684,611

Applicant(s)

MEYNANTS, GUY

Examiner

Heather R. Long

Art Unit

2615

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 December 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-25 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 06 October 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 4/1/2002.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

1. Applicant's election with traverse of the amplifying circuit in the reply filed on 12/6/2004 is acknowledged. The traversal is on the ground(s) that all the species illustrate an amplifying circuit for a pixel array in an imaging device and that the same reference numbers are used through the different embodiments. This is not found persuasive because each embodiment has different characteristics that are unique to that particular embodiment, which create a burdensome search on the examiner. Furthermore, the Applicant has failed to prove that these characteristics would not create be a burdensome search. Therefore, the requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Dierickx et al. (WO 99/16238).

Regarding claim 1, Dierickx et al. discloses in Fig. 2 an amplifying circuit, comprising: an amplifying element (A1) with at least an input terminal and an output terminal, a signal input node (I1), the signal levels of which at least two moments in time are to be amplified by the amplifying element (page 11, lines 6-

9), at least two connecting lines between the signal input node and the amplifying element (these lines can be seen in Fig. 2), for transferring a signal from the signal input node to the input terminal of the amplifying element, a memory element (MR1 or MS1) on at least one of the connecting lines, for storing a signal level of the signal input node at a moment in time (page 11, lines 15-27), a switching element disposed on each connecting line (S41 and S51), between the memory element and the input terminal of the amplifying element if a memory element is provided on the connecting line, for consecutively connecting signal levels of the signal input node at different moments in time to the same amplifying element, at least one output node (can be seen in Fig. 2), each output node being connected to the output terminal of the same amplifying element.

Regarding claim 2, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 1 as well as disclosing that the amplifying circuit comprises a memory element on each of the connecting lines (MR1 and MS1).

Regarding claim 3, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 1 including that there are the same number of output nodes as there are connecting lines (as can be seen in Fig. 2, there is one output line and one connecting line), output nodes and connecting lines being associated with each other according to a 1 to 1 relationship, each output node being consecutively connected over the same amplifying element to the connecting line with which it is associated (this can be seen in Fig. 2).

Regarding claims 4 and 5, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 1 including that the amplifying element is a transistor or a transistor of the type of metal oxide semiconductor transistors. (It is inherent that the amplifying element is a transistor or a transistor of the type of metal oxide semiconductor transistors).

Regarding claim 6, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 1 including that the amplifying element is an operational transconductance amplifier (It is inherent that the amplifying element is an operational transconductance amplifier).

Regarding claim 7, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 1 including that the memory element is a capacitor (page 11, lines 20-21 and 27).

Regarding claim 8, Dierickx et al. discloses in Fig. 2 an array of amplifying circuits, each amplifying circuit, comprising: an amplifying element (A1) with at least an input terminal and an output terminal, a signal input node (I1), the signal levels of which at least two moments in time are to be amplified by the amplifying element (page 11, lines 6-9), at least two connecting lines between the signal input node and the amplifying element (these lines can be seen from Fig. 2), for transferring a signal from the signal input node to the input terminal of the amplifying element, a memory element (MR1 or MS1) on at least one of the connecting lines, for storing a signal level of the signal input node at a moment in time (page 11, lines 15-27), a switching element disposed on each connecting

line (S41 and S51), between the memory element and the input terminal of the amplifying element if a memory element is provided on the connecting line, for consecutively connecting signal levels of the signal input node at different moments in time to the same amplifying element, at least one output node (can be seen in Fig. 2), each output node being connected to the output terminal of the same amplifying element, the array further comprising: at least one output line (Y) in common to all amplifying circuits of the array, the output nodes of the amplifying circuits being connected to the output lines.

Regarding claim 9, Dierickx discloses in Fig. 2 a device for imaging applications, comprising: a matrix of active pixels arranged in a geometric configuration, each pixel producing an electrical signal indicative of the light intensity of a portion of a scene being imaged by that pixel (page 1, lines 25-32), at least one amplifying circuit common to a group of pixels out of the matrix, at least one output line wherein each amplifying circuit comprises an amplifying element (A1) with at least an input terminal and an output terminal, a signal input node (I1) being intended to obtain electrical signals from pixels out of the group of pixels to which the amplifying circuit is common, the signal levels of are to be amplified by the amplifying element (page 11, lines 6-9), at least two connecting lines between the signal input node and the amplifying element (these lines can be seen in Fig. 2), for transferring an electrical signal from the signal input node to the input terminal of the amplifying element, a memory element (MR1 or MS1) on at least one of the connecting lines, for storing a signal level of the electrical

signals at the signal input node at a moment in time (Page 11, lines 15-27), a switching element disposed on each connecting line, between the memory element and the input terminal of the amplifying element if a memory element is provided on the connecting line (S41 and S51), for consecutively connecting signal levels of the signal input node at different moments in time to the same amplifying element, at least one output node (can be seen in Fig. 2), each output node being connected to the output terminal of the same amplifying element.

Regarding claim **10**, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 9 including that the matrix is arranged in columns and rows and wherein the group of pixels is a row of pixels (Fig. 2).

Regarding claim **11**, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 9 including that the matrix is arranged in columns and rows and wherein the group of pixels is a column of pixels (Fig. 2).

Regarding claim **12**, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 9 including that the output lines (I1) are common to the matrix of active pixels, the output node of each amplifying circuit being connected to the output lines (Y).

Regarding claim **13**, Dierickx et al. discloses all the limitations as previously discussed with respect to any of the claims 9-12 as well as disclosing that the device may be used in camera systems or imaging applications requiring a high image quality (page 1, lines 15-19).

Regarding claim **14**, Dierickx et al. discloses a pixel adapted for integration in an imaging device, comprising: a radiation sensitive element able to produce an electrical signal indicative of the amount of radiation picked up by that pixel (page 1, lines 25-32), an amplifying circuit wherein the amplifying circuit comprises an amplifying element (A1) with at least an input terminal and an output terminal, a signal input node (I1), the signal levels of which at least two moments in time are to be amplified by the amplifying element the signal levels being obtained from the radiation sensitive element (page 11, lines 6-9), at least two connecting lines between the signal input node and the amplifying element (these lines can be seen in Fig. 2), for transferring a signal from the signal input node to the input terminal of the amplifying element, a memory element (MR1 or MS2) on at least one of the connecting lines, for storing a signal level of the signal input node at a moment in time (page 11, lines 15-27), a switching element disposed on each connecting line (S41 and S51), between the memory element and the input terminal of the amplifying element if a memory element is provided on the connecting line, for consecutively connecting signal levels of the signal input node at different moments in time to the same amplifying element, at least one output node (can be seen in Fig. 2), each output node being connected to the output terminal of the same amplifying element.

Regarding claim **15**, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 14 including that the radiation sensitive element is a photodiode (page 1, lines 25-32).

Regarding claim **16**, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 14 including that the radiation sensitive element is an infrared photodetector (page 1, lines 25-32).

Regarding claim **17**, Dierickx et al. discloses a method for reducing fixed pattern noise of solid state imaging device having a group of active pixels (page 4, lines 30-35), each pixel comprising a radiation sensitive element (page 1, lines 25-32) and an amplifying circuit, the method comprising the following steps: reading out the signal of a pixel brought in a first state and storing the corresponding voltage level in a first memory element, reading out the signal of the pixel brought in a second state (which is different from the first state) and storing the corresponding voltage level in a second memory element (page 11, lines 15-28), transferring the signal of the first memory element to an amplifying element, amplifying it and transferring it to an output line, transferring the signal of the second memory element to the same amplifying element, amplifying it and transferring it to an output line, repeating these steps for at least part of the pixels of the imaging device (page 11, line 29 – page 12, line 8).

Regarding claim **18**, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 17 including that the memory element uses one output line (can be seen in Fig. 2).

Regarding claim **19**, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 17 as well as disclosing that it further

comprises the step of calculating a differential output signal by taking the difference between potential values on the output lines (page 3, lines 10-23).

Regarding claim **20**, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 17 including that the first state and the second state correspond to different amounts of radiation collected on the radiation sensitive element in the pixel (page 11, lines 15-28).

Regarding claim **21**, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 20 including that the first state or second state corresponds to an amount of radiation or light collected on the radiation sensitive element in the pixel (page 11, lines 15-28).

Regarding claim **22**, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 20 including that the second state or the first state corresponds to a non-irradiated or non-illuminated or dark or reset state of the pixel (page 11, lines 15-28).

Regarding claim **23**, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 17 including that the pixel is read out in additional states and its corresponding voltage level is being stored on additional memory elements (page 1, line 25 – page 4 lines 7; page 11, lines 6 – page 12, line 20).

Regarding claim **24**, Dierickx et al. discloses all the limitations as previously discussed with respect to claim 17 including that the signal of the first memory element is transferred to the first output line common for the group, and

concurrently, the signal of the second memory element of another amplifier is transferred to the second output line common for the group (Fig. 3).

Regarding claim **25**, Dierickx discloses a method for reducing fixed pattern noise and kTC noise in a solid state imaging device having a group of active pixels (page 10, lines 29-35), each pixel comprising a radiation sensitive element (page 1, lines 25-32) and an amplifying circuit, the method comprising the following steps: reading out the signal of a pixel brought in a first state, corresponding to the non-illuminated or dark condition of the pixel or to the reset state of the pixel, and storing the corresponding voltage level alternately on a first or a third memory element, reading out the signal of the pixel in a second state, at a later moment in time, corresponding to an amount of radiation or light collected on the radiation sensitive element on the pixel, and storing the corresponding voltage level on a second memory element alternately (page 11, lines 15-27), transferring the signal of the first or third memory element to an amplifying element, amplifying it and transferring it to an output line that is common to the group of pixels, transferring the signal of the second memory element to the same amplifying element, amplifying it and transferring it to an output line that is common to the group of pixels, repeating this operation for essentially all or part of the pixels of the imaging device (page 11, line 29 – page 12, line 8).

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Conclusion


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Heather R. Long whose telephone number is 571-272-7368. The examiner can normally be reached on Mon. - Thurs.: 7:00 am - 4:30 pm, and every other Fri.: 7:00 am - 3:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, James Groody can be reached on 571-272-7950. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Heather R Long
Examiner
Art Unit 2615

HRL
May 2, 2005


TUAN HO
PRIMARY EXAMINER